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10CS74

Seventh Semester B.E. Degree Examination, May 2017
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. What is dependability? Explain two main measures of dependability. **(06 Marks)**

c. A compiler designer is trying to describe between two code sequence for a particular high level language statement. Consider two code sequences that require the following instruction counts.

Code sequence	Instruction counts for Instruction class		
	A	B	C
1	2	1	2
2	4	1	1

(i) Which code sequence executes of the instruction?
(ii) What is the CPI for each sequence?
(iii) Which will be faster? **(06 Marks)**

2 a. Explain different techniques in reducing pipeline branch penalties. **(06 Marks)**

b. What are the major hazards in a pipeline? Explain data hazard and methods to minimize data hazard with example. **(08 Marks)**

c. List and explain the requirements on expetion. **(06 Marks)**

3 a. What are the basic compiler techniques for exposing ILP? Explain briefly. **(06 Marks)**

b. Explain with a neat diagram of basic structure of Tomosulo based Mips FP units. **(07 Marks)**

c. What are dependencies? Explain with example. **(07 Marks)**

4 a. Explain the issues in implementing advanced speculation. **(09 Marks)**

b. Explain with neat diagram Pentium 4 pipeline supporting multiple issues with speculation. **(08 Marks)**

c. Write note on Branch target buffer. **(03 Marks)**

PART – B

5 a. What is multiprocessor cache coherence? Illustrate the problem and show how different processors have different value for the same location. **(08 Marks)**

b. Explain the different taxonomy of parallel architecture. **(08 Marks)**

c. Write a note on Spin lock. **(04 Marks)**

6 a. Explain the six basic cache optimization. **(09 Marks)**

b. Explain with a diagram the organization of data cache in the opteron microprocessor. **(08 Marks)**

c. Difference between page versus segment. **(03 Marks)**

7 a. Which are the major categories of advanced optimization of cache performance? Explain any two. **(10 Marks)**

b. Explain internal organization of 64 kB DRAM with a diagram. **(05 Marks)**

c. Write a note on virtual machine. **(05 Marks)**

8 a. Explain detecting and enhancing loop level parallelism for VLIW. **(08 Marks)**

b. Explain Intel IA-64 Architecture. **(08 Marks)**

c. What are the four methods for supporting exception behavior without erroneous. **(04 Marks)**

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